

PXI  
CompactPCI  
CAN  
Industrial Platform  
ICT  
Functional Test

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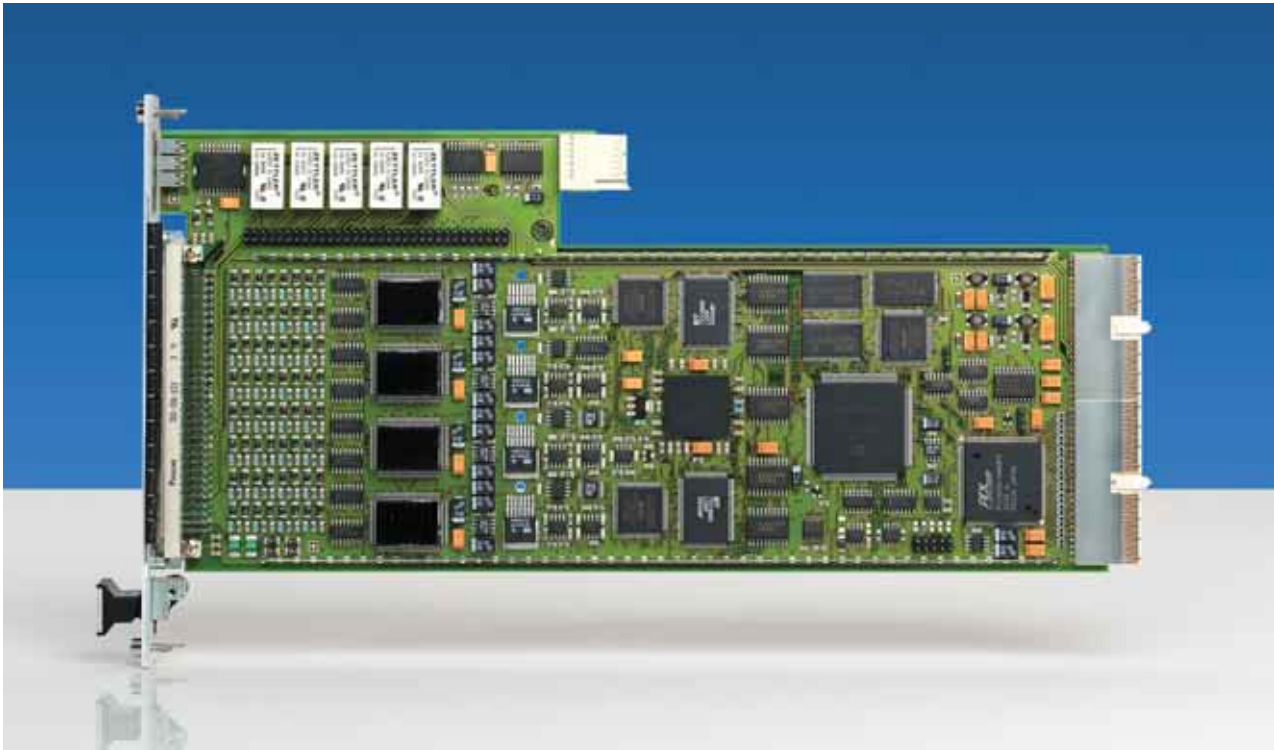
## Digital Functional Test Module R&S® TS-PDFT

High-speed 32-bit digital pattern I/O and serial communications interfaces

- ◆ 32 digital output channels in four groups
- ◆ Pattern rate 20 MHz
- ◆ One programmable output level per group
- ◆ High output current
- ◆ Short-circuit protection
- ◆ Stimulation of digital realtime data, streams with variable bus width
- ◆ Four high power open drain channels, fully protected, capable of pulse width modulation
- ◆ Five relay channels SPST
- ◆ 32 digital input channels in four groups
- ◆ Two programmable input threshold levels per group for hysteresis or level monitoring
- ◆ Acquisition of digital realtime data streams with variable bus width
- ◆ Overvoltage protection
- ◆ Serial communications interfaces
  - CAN 2.0b high-speed
  - CAN 2.0b low-speed, fault-tolerant
  - RS-232-C / K bus
  - SPI bus emulation (master)
  - I<sup>2</sup>C bus emulation (master)
- ◆ Local microprocessor
- ◆ For time-critical tasks independent of the operating system used
- ◆ Synchronization via PXI trigger bus
- ◆ Software front panels for immediate use
- ◆ Selftest software
- ◆ LabWindows/CVI device driver support
- ◆ Test software library GTSL in DLL format



**ROHDE & SCHWARZ**



## Product introduction

The Digital Functional Test Module R&S®TS-PDFT is a CompactPCI/PXI module which takes up only one slot in the R&S®CompactTSVP (Test System Versatile Platform). The module contains very flexibly programmable 32-bit digital inputs and 32-bit digital outputs which are able to acquire or stimulate static or dynamic digital patterns. The characteristics of the digital lines can be configured in 8-bit ports. Furthermore, the programmable levels of the output ports can be adjusted to the application requirements, and the input ports have a programmable threshold and hysteresis to match the specifications of common digital logic families.

The synchronization to digital communications, handshake signals and analog measurement tasks is provided via trigger lines accessible at the front connector or via the PXI trigger lines. Additionally, the module can generate trigger-pulses derived from digital pattern com-

parisons and perform change detection at the input ports.

The scope of the R&S®TS-PDFT's digital I/O capabilities is supported by the on-board microprocessor which can provide various communications interfaces, especially suited for automotive applications.

The simulation of the DUT's environment is simplified by providing floating relays to switch supply voltages or loads to the DUT. With four additional power-output channels that can be pulse-width-modulated, digital control signals with up to 1 A can be applied to the test setup via open drain switching outputs.

The digital channels are equipped with protection circuits and signal conditioning features to use the Digital Functional Test Module R&S®TS-PDFT as a robust device for various tasks in automatic test equipment (ATE), thus covering a wide scope of measurement and control objectives.

## Typical applications

The Digital Functional Test Module R&S®TS-PDFT can be used in all test and measurement scenarios where simple or complex digital circuits have to be tested by static or dynamic digital patterns. The feature of DUT programming in production provides a very efficient approach to testing and uploading firmware to the DUTs in one step in the test process.

For many applications, realistic simulation of the DUT's environment during testing is most important.

The R&S®TS-PDFT therefore offers deterministic generation and simultaneous acquisition of digital patterns at high data rates. This includes both tristate control and the implementation of bidirectional buses by configuring portwise connections of input and output lines by software. These test setups can be even operated in correlation with a realtime communications path based on standardized interfaces.

For automotive ATE, the most common interfaces are SPI, I<sup>2</sup>C, CAN, K bus or RS-232-C which are supported by the R&S®TS-PDFT.

Further applications are related to various programming tasks that have to be performed by state-of-the-art board test systems. The R&S®TS-PDFT can handle most common programming procedures for downloading to flash memories and transferring data streams to on-board memory.

The on-board computing power provides firmware-implemented communications protocols and supports communications tasks that are time-critical or that need realtime response independently of the operating system that is running on the R&S®CompactTSVP's system controller.

A sophisticated set of trigger setups provides flexible synchronization to DUT signals or synchronizes to multiple R&S®TS-PDFT modules, Rohde & Schwarz measurement modules or commercially available PXI modules via the standardized PXI trigger bus.

Typical applications include:

- ◆ Digital functional test
- ◆ Interfacing to digital communications
- ◆ Downloading to flash memories
- ◆ Deterministic stimulation and acquisition of digital data streams
- ◆ Digital I/O control
- ◆ Simulation of digital bus lines

## Flexibility

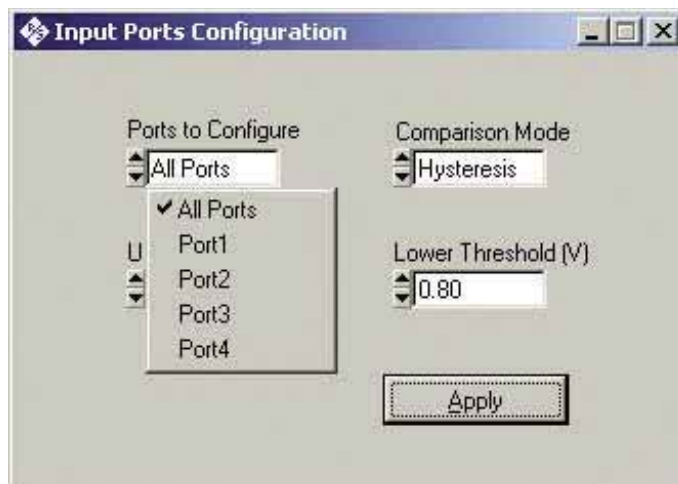
The design of the module offers expanded flexibility for various application scenarios and high-speed pattern I/O. The programmability of the digital I/O interfaces enables the module to meet a wide range of requirements regarding data transfer, communications and trigger settings. The features are contained in the free software front panels and are available for immediate use.

The programmable output levels and input threshold levels of the configurable ports ensure compatibility with future generations of digital components.

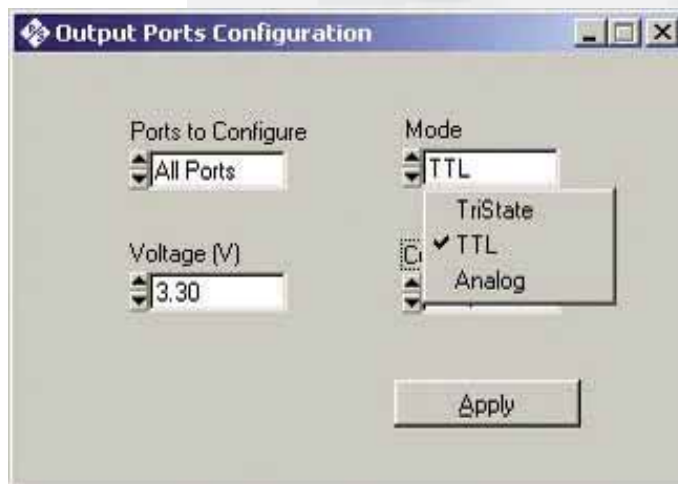
To improve noise immunity in test environments, the hysteresis of the input channels can be configured groupwise.

If a higher number of digital I/O lines is required, multiple R&S®TS-PDFT modules can be synchronized within the system or synchronized with other types of measurements via the PXI trigger bus.

To simplify update procedures, the firmware for the microcontroller and the on-board FPGA design can be easily downloaded. This allows the R&S®TS-PDFT's firmware to be upgraded with new functionalities or enhancements.



*Configuration of input ports*



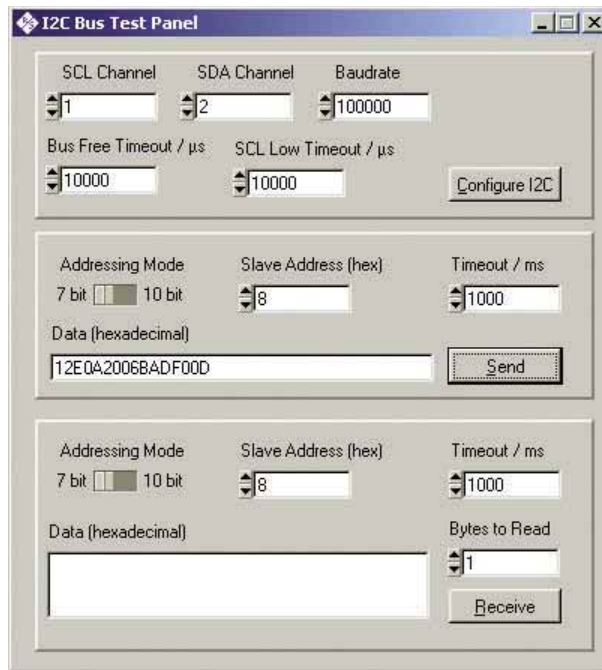
*Configuration of output ports*

## Software support

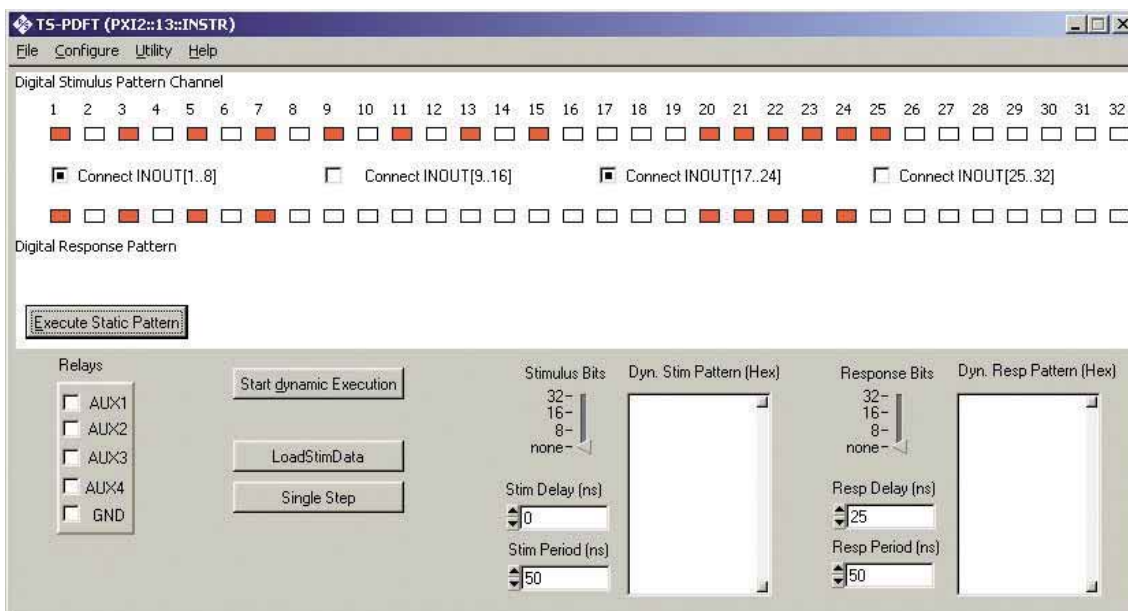
A LabWindows/CVI driver for standardized device operation is available for the R&S®TS-PDFT. Function panels and on-line help are available as common features for the LabWindows/CVI driver.

The definition and evaluation of complex digital test scenarios are supported by the Rohde & Schwarz GTSL (Generic Test Software Library) software including the DIO manager.

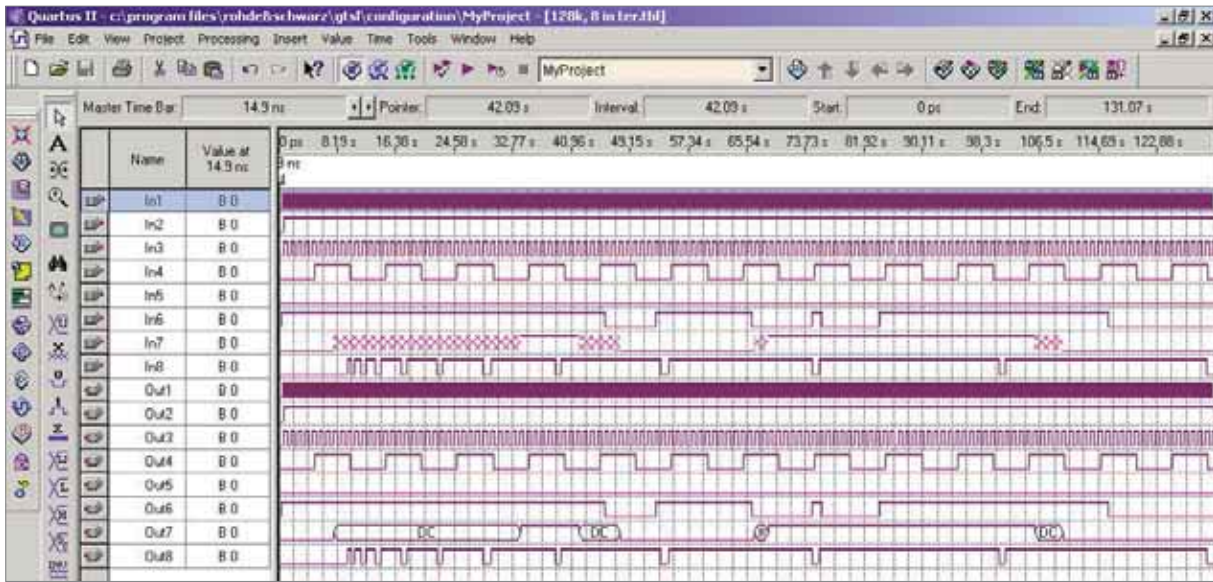
A set of software front panels makes it easy for users to learn the module's various functionalities. The software front panels also include features for evaluating serial communications protocols. This allows users to evaluate test setups simply by using test panels rather than by means of programming.



*I<sup>2</sup>C bus test panel*



*Static digital I/O loopback*



*Quartus II software for creating and displaying digital stimulation patterns*

The Quartus® II Web Edition software from Altera® is a highly sophisticated tool for creating programmable logic designs. It also provides a convenient means of generating digital pattern sets and is also suitable for visualizing digital patterns that were acquired using the R&S®TS-PDFT.

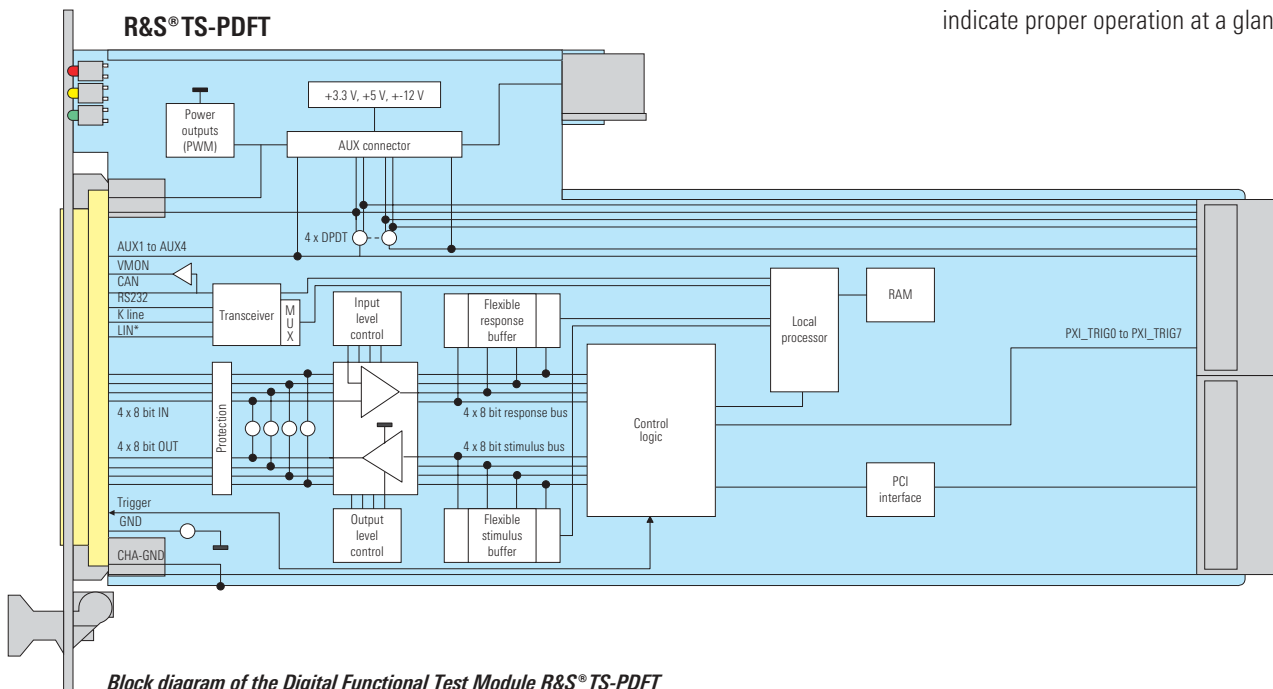
Waveform data can be loaded into and retrieved from the module's on-board memory by means of driver functions provided by the DIO manager library, which is part of the Rohde & Schwarz GTSL software package.

The driver functionality also covers the synchronization of multiple modules and pattern sets.

### Security through selftest and diagnostics

The built-in selftest capability of the module and the related selftest application ranges from fast diagnostics to the complete, automated evaluation of output levels, trigger lines and all switching paths.

Diagnostic LEDs on the module front panel speed up system integration and indicate proper operation at a glance.



*Block diagram of the Digital Functional Test Module R&S®TS-PDFT*

## Specifications

Application in R&S®TSVP platform	
R&S®CompactTSVP	1 slot required
Interface	
Control bus	CompactPCI/PXI
DUT connector (front)	DIN 41612, 96 pins
Rear I/O connector	CompactPCI, 110 pins
Data input channels	
Channels	32, in 4 groups of 8 bits
Input modes <sup>1)</sup>	hysteresis comparator
Input level	-5 V to +12 V clamping if outside range
Input thresholds <sup>1)</sup>	two programmable thresholds 0 V to +9.5 V at 12-bits resolution
Input resistance	1 M $\Omega$
Realtime acquisition	
Sample rate	0.01 Hz to 20 MHz with 25 ns resolution
Trigger delay	0 s to 100 s with 25 ns resolution
Data buffer depth / width (programmable)	131071 samples at 8 bits (IN 1 to 8) 65535 samples at 16 bits (IN 1 to 16) 32768 samples at 32 bits (IN 1 to 32)
Protection	overvoltage protection $\pm 42$ V (max. 60 V <30)
Data output channels	
Channels	32, in 4 groups of 8 bits
Output modes	TTL, analog, tristate
TTL output mode <sup>1)</sup>	
Output voltage	$V_{OH} = \text{max. } +3.3$ V $V_{OH} = \text{typ. } +2.5$ V at 20 mA $V_{OL} = \text{typ. } +0.8$ V at 20 mA max. 80 mA
Output current	
Analog output mode <sup>1)</sup>	
Output voltage	-3 V to 10 V
Output current	max. 150 mA per channel, 10 mA to 700 mA per group <sup>1)</sup>
Output resolution	12 bits
Tristate control output mode	
Output voltage	none
Output resistance	typ. 39 $\Omega$
Realtime stimulation <sup>1)</sup>	
Sample rate	0.01 Hz to 20 MHz at 25 ns resolution
Trigger delay	100 ns to 100 s at 25 ns resolution
Data buffer depth / width (programmable)	131071 samples at 8 bits (OUT 1 to 8) 65535 samples at 16 bits (OUT 1 to 16) 32768 samples at 32 bits (OUT 1 to 32)
Tristate control	programmable, per sample
Implementation of bidirectional data buses	portwise connection of data output with data input channels via on-board analog switches
Protection	short circuit reverse voltage up to $\pm 42$ V at 150 mA
Power output channels	

Channels	4, open drain
Maximum switching voltage	+45 V
Maximum switching current	1 A per channel
Pulse width modulation (PWM)	1 Hz to 40 kHz at 0 % to 100 % duty cycle
Protection	short circuit, overvoltage, overtemperature
Relay channels	
Channels	4, SPST, floating 1, SPST, to ground
Maximum switching voltage DC/AC	60 V / 42 V rms
Maximum switching current DC/AC	1.5 A / 1.5 A rms
Maximum switching power DC/AC	100 W / 100 VA
Communications interfaces	
CAN interface	
Channels	1 (microprocessor, full CAN) CAN 2.0B active, 11/29-bit identifier
Modes	low-speed, fault-tolerant (ISO11519-2) up to 125 kbd, transceiver TJA1054 high-speed (ISO11898) up to 1 Mbd, transceiver PCA82C251 programmable
Termination	programmable
TX objects	4, Software-FIFO-buffered
RX objects	11, programmable filters, Software-FIFO-buffered
Cyclic TX messages	2, independent frame bursts, Software-FIFO-buffered, programmable cycle time
Asynchronous serial interface	
Channels	1 (microprocessor, UART)
Modes	RS-232-C, K bus, TTL (uses XTI and XTO)
Transfer rates	110 bit/s to 115 bit/s
Data formats	1 start bit 7 data bits with even/odd parity 8 data bits with/without even/odd parity 9 data bits 1 or 2 stop bits
SPI interface	
Channels	emulation of bus master via data channels used outputs: 3 (CLK, MOSI, CS) used inputs: 1 (MISO)
Modes	4
Transfer rate	100 bit/s to 300 kbit/s
Data formats	1 bit to 32 bit
I <sup>2</sup> C interface	
Channels	emulation of bus master via data channels <sup>2)</sup> outputs used: 2 (I <sup>2</sup> C_SCL, I <sup>2</sup> C_SDA) inputs used: 2 (I <sup>2</sup> C_SCL, I <sup>2</sup> C_SDA)
Modes	7-bit and 10-bit addressing
Transfer rate	50 bit/s to 300 kbit/s
Pattern comparator	
Comparison	32-bit data input channels with 32-bit reference pattern 32-bit comparison enable mask

Application	
Frequency measurement <sup>3)</sup>	
Maximum input frequency	12.5 MHz at 50 % duty cycle
Minimum pulse width	40 ns
Frequency resolution	25 ns
Measurement time	100 s to 160 ns gate time or up to 65534 comparator matches
Trigger	software trigger
Application	
Event counting <sup>3)</sup>	
Minimum pattern duration	40 ns
Gate time	100 s to 160 ns
Event counts	up to 65534
Application trigger generator	output to PXI trigger, XTO input to trigger units
<b>Realtime control unit</b>	
Local microprocessor	ST10F269 16-bit 40 MHz 2 Mbyte RAM
<b>Synchronization</b>	
Trigger units	2, fully independent hardware trigger logic
Applications	programmable trigger generator generation of realtime stimulation clock generation of realtime acquisition clock frequency measurement
Trigger unit characteristics <sup>4)</sup>	2, fully independent hardware trigger logic
Input signals	1, local TTL trigger (XTI) 8, PXI trigger bus
Reference pattern	1, pattern comparator
Slope	10-bit, 3 states: high, low, don't care
Delay	positive / negative
Output signals	40 ns to 100 s trigger received signal (25 ns pulse) trigger active signal (start of trigger until burst end) sample pulse (25 ns pulse for each sample)
Synchronization outputs	
Channels	1, local TTL trigger (XTO) 8, PXI trigger bus
Signals <sup>5)</sup>	output trigger unit 1 (IT1) output trigger unit 2 (IT2) output pattern comparator input signal (XTI)

## General data

Power consumption	+3.3 V / 0.5 A, +5 V / 1.6 A, +12 V / 0.4 to 2.4 A, -12 V / 0.1 A
EMC compliance	compliant with EMC directive 89/336/EEC and EMC standard EN 61326
Safety	CE, EN 61010 Part 1
<b>Mechanical loading</b>	
Vibration test, sinusoidal	5 Hz to 55 Hz: 2 g, MIL-T-28800D, class 5, 55 Hz to 150 Hz: 0.5 g, MIL-T-28800D, class 5
Vibration test, random	10 Hz to 300 Hz, 1.2 g
Shock test	40 g, MIL-STD-810, classes 3 and 5
<b>Temperature loading</b>	
Operating temperature range	+5 °C to +40 °C
Permissible temperature range	0 °C to +50 °C
Storage temperature range	-40 °C to +70 °C
Humidity	+40 °C, 95 % rel. humidity
Dimensions	316 mm × 174 mm × 20 mm
Weight	0.37 kg

<sup>1)</sup> programmable per group.

<sup>2)</sup> external diodes and pull-up resistors required.

<sup>3)</sup> uses one trigger unit.

<sup>4)</sup> programmable per trigger unit.

<sup>5)</sup> selectable per synchronization channel.

## Ordering information

Designation	Type	Order No.
Digital Functional Test Module	R&S®TS-PDFT	1143.0080.02
Open Test Platform R&S®CompactTSVP	R&S®TS-PCA3	1152.2518.02

More information at  
[www.rohde-schwarz.com](http://www.rohde-schwarz.com)  
(search term: TS-PDFT)



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